



# 256K x 16-Bit 3.3-V Asynchronous Magnetoresistive RAM

## MR2A16A



44-TSOP  
Case 924A-02

### Introduction

The MR2A16A is a 4,194,304-bit magnetoresistive random access memory (MRAM) device organized as 262,144 words of 16 bits. The MR2A16A is equipped with chip enable ( $\overline{E}$ ), write enable ( $\overline{W}$ ), and output enable ( $\overline{G}$ ) pins, allowing for significant system design flexibility without bus contention. Because the MR2A16A has separate byte-enable controls ( $\overline{LB}$  and  $\overline{UB}$ ), individual bytes can be written and read.

MRAM is a nonvolatile memory technology that protects data in the event of power loss and does not require periodic refreshing. The MR2A16A is the ideal memory solution for applications that must permanently store and retrieve critical data quickly.

The MR2A16A is available in a 400-mil, 44-lead plastic small-outline TSOP type-II package with an industry-standard center power and ground SRAM pinout.

The MR2A16A is available in Commercial (0°C to 70°C), Industrial (-40°C to 85°C) and Extended (-40°C to 105°C) ambient temperature ranges.

### Features

- Single 3.3-V power supply
- Commercial temperature range (0°C to 70°C), Industrial temperature range (-40°C to 85°C) and Extended temperature range (-40°C to 105°C)
- Symmetrical high-speed read and write with fast access time (35 ns)
- Flexible data bus control — 8 bit or 16 bit access
- Equal address and chip-enable access times
- Automatic data protection with low-voltage inhibit circuitry to prevent writes on power loss
- All inputs and outputs are transistor-transistor logic (TTL) compatible
- Fully static operation
- Full nonvolatile operation with 20 years minimum data retention

## Device Pin Assignment

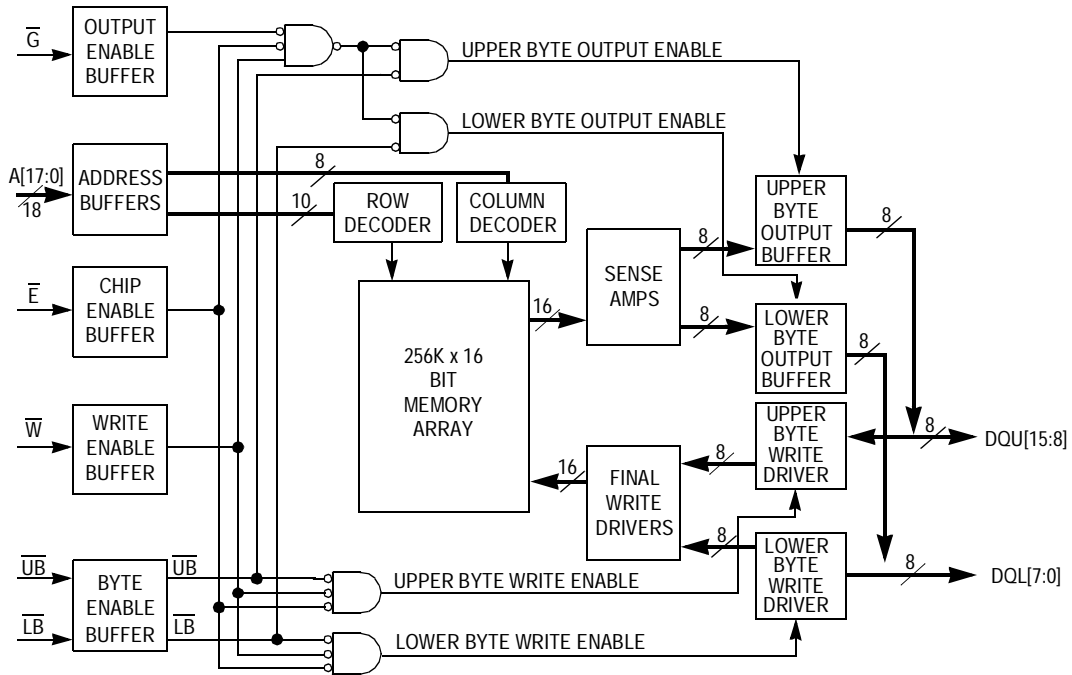


Figure 1. Block Diagram

## Device Pin Assignment

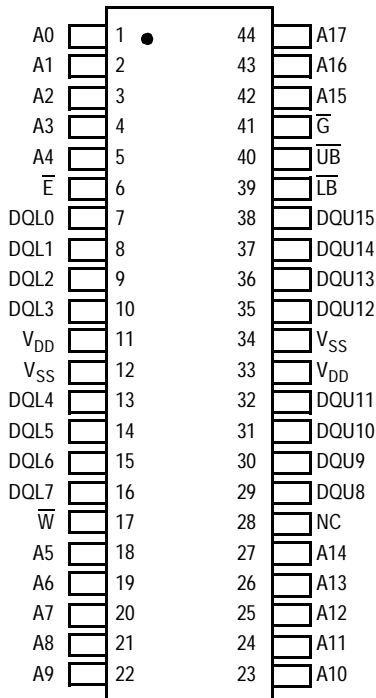


Table 1. Pin Functions

Signal Name	Function
A	Address input
$\bar{E}$	Chip enable
$\bar{W}$	Write enable
$\bar{G}$	Output enable
$\bar{UB}$	Upper byte select
$\bar{LB}$	Lower byte select
DQL	Data I/O, lower byte
DQU	Data I/O, upper byte
$V_{DD}$	Power supply
$V_{SS}$	Ground
NC	Do not connect this pin

Figure 2. MR2A16A in 44-Pin TSOP Type II Package

Table 2. Operating Modes

$\overline{E}^1$	$\overline{G}^1$	$\overline{W}^1$	$\overline{LB}^1$	$\overline{UB}^1$	Mode	$V_{DD}$ Current	DQL[7:0] <sup>2</sup>	DQU[15:8] <sup>2</sup>
H	X	X	X	X	Not selected	$I_{SB1}, I_{SB2}$	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	$I_{DDR}$	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	$I_{DDR}$	Hi-Z	Hi-Z
L	L	H	L	H	Lower byte read	$I_{DDR}$	$D_{Out}$	Hi-Z
L	L	H	H	L	Upper byte read	$I_{DDR}$	Hi-Z	$D_{Out}$
L	L	H	L	L	Word read	$I_{DDR}$	$D_{Out}$	$D_{Out}$
L	X	L	L	H	Lower byte write	$I_{DDW}$	$D_{In}$	Hi-Z
L	X	L	H	L	Upper byte write	$I_{DDW}$	Hi-Z	$D_{In}$
L	X	L	L	L	Word write	$I_{DDW}$	$D_{In}$	$D_{In}$

## NOTES:

<sup>1</sup> H = high, L = low, X = don't care

<sup>2</sup> Hi-Z = high impedance

## Electrical Specifications

### Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 3. Absolute Maximum Ratings<sup>1</sup>

Parameter	Symbol	Value	Unit
Supply voltage <sup>2</sup>	$V_{DD}$	-0.5 to 4.0	V
Voltage on any pin <sup>2</sup>	$V_{In}$	-0.5 to $V_{DD} + 0.5$	V
Output current per pin	$I_{Out}$	$\pm 20$	mA
Package power dissipation <sup>3</sup>	$P_D$	0.600	W
Temperature under bias MR2A16ATS35C (Commercial - Legacy) MR2A16AYS35 (Commercial - New) MR2A16ACYS35 (Industrial) MR2A16AVYS35 (Extended)	$T_{Bias}$	-10 to 85 -10 to 85 -45 to 95 -45 to 110	°C
Storage temperature	$T_{stg}$	-55 to 150	°C
Lead temperature during solder (3 minute max)	$T_{Lead}$	260	°C
Maximum magnetic field during write MR2A16ATS35C (Commercial - Legacy) MR2A16AYS35 (Commercial - New) MR2A16ACYS35 (Industrial) MR2A16AVYS35 (Extended)	$H_{max\_write}$	15 25 25 25	Oe
Maximum magnetic field during read or standby	$H_{max\_read}$	100	Oe

## NOTES:

- <sup>1</sup> Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
- <sup>2</sup> All voltages are referenced to  $V_{SS}$ .
- <sup>3</sup> Power dissipation capability depends on package characteristics and use environment.

Table 4. Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage					
MR2A16ATS35C (Commercial - Legacy)	$V_{DD}$	3.0 <sup>1</sup>	3.3	3.6	V
MR2A16AYS35 (Commercial - New)		3.0 <sup>2</sup>	3.3	3.6	
MR2A16ACYS35 (Industrial)		3.0 <sup>2</sup>	3.3	3.6	
MR2A16AVYS35 (Extended)		3.0 <sup>2</sup>	3.3	3.6	
Write inhibit voltage					
MR2A16ATS35C (Commercial - Legacy)	$V_{WI}$	2.5	2.7	3.0 <sup>1</sup>	V
MR2A16AYS35 (Commercial - New)		2.5	2.7	3.0 <sup>2</sup>	
MR2A16ACYS35 (Industrial)		2.5	2.7	3.0 <sup>2</sup>	
MR2A16AVYS35 (Extended)		2.5	2.7	3.0 <sup>2</sup>	
Input high voltage	$V_{IH}$	2.2	—	$V_{DD} + 0.3$ <sup>3</sup>	V
Input low voltage	$V_{IL}$	-0.5 <sup>4</sup>	—	0.8	V
Operating temperature					
MR2A16ATS35C (Commercial - Legacy)	$T_A$	0		70	°C
MR2A16AYS35 (Commercial - New)		0		70	
MR2A16ACYS35 (Industrial)		-40		85	
MR2A16AVYS35 (Extended)		-40		105	

## NOTES:

- <sup>1</sup> After power up or if  $V_{DD}$  falls below  $V_{WI}$ , a waiting period of 2  $\mu$ s must be observed, and  $\overline{E}$  and  $\overline{W}$  must remain high for 2  $\mu$ s. Memory is designed to prevent writing for all input pin conditions if  $V_{DD}$  falls below minimum  $V_{WI}$ .
- <sup>2</sup> After power up or if  $V_{DD}$  falls below  $V_{WI}$ , a waiting period of 2 ms must be observed, and  $\overline{E}$  and  $\overline{W}$  must remain high for 2 ms. Memory is designed to prevent writing for all input pin conditions if  $V_{DD}$  falls below minimum  $V_{WI}$ .
- <sup>3</sup>  $V_{IH}(\text{max}) = V_{DD} + 0.3 \text{ Vdc}$ ;  $V_{IH}(\text{max}) = V_{DD} + 2.0 \text{ Vac}$  (pulse width  $\leq 10 \text{ ns}$ ) for  $I \leq 20.0 \text{ mA}$ .
- <sup>4</sup>  $V_{IL}(\text{min}) = -0.5 \text{ Vdc}$ ;  $V_{IL}(\text{min}) = -2.0 \text{ Vac}$  (pulse width  $\leq 10 \text{ ns}$ ) for  $I \leq 20.0 \text{ mA}$ .

## Electrical Specifications

### Direct Current (dc)

**Table 5. dc Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current	$I_{Ikg(I)}$	—	—	$\pm 1$	$\mu A$
Output leakage current	$I_{Ikg(O)}$	—	—	$\pm 1$	$\mu A$
Output low voltage ( $I_{OL} = +4 \text{ mA}$ ) ( $I_{OL} = +100 \mu A$ )	$V_{OL}$	—	—	0.4 $V_{SS} + 0.2$	V
Output high voltage ( $I_{OH} = -4 \text{ mA}$ ) ( $I_{OH} = -100 \text{ mA}$ )	$V_{OH}$	2.4 $V_{DD} - 0.2$	—	—	V

**Table 6. Power Supply Characteristics**

Parameter	Symbol	Typ	Max	Unit
ac active supply current — read modes <sup>1</sup> ( $I_{Out} = 0 \text{ mA}$ , $V_{DD} = \text{max}$ )	$I_{DDR}$	55	80	mA
ac active supply current — write modes <sup>1</sup> ( $V_{DD} = \text{max}$ ) MR2A16ATS35C (Commercial - Legacy) MR2A16AYS35 (Commercial - New) MR2A16ACYS35 (Industrial) MR2A16AVYS35 (Extended)	$I_{DDW}$	105 105 105 105	155 155 165 165	mA
ac standby current ( $V_{DD} = \text{max}$ , $\bar{E} = V_{IH}$ ) (no other restrictions on other inputs)	$I_{SB1}$	18	28	mA
CMOS standby current ( $\bar{E} \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$ ) ( $V_{DD} = \text{max}$ , $f = 0 \text{ MHz}$ )	$I_{SB2}$	9	12	mA

NOTES:

<sup>1</sup> All active current measurements are measured with one address transition per cycle.

**Table 7. Capacitance<sup>1</sup>**

Parameter	Symbol	Typ	Max	Unit
Address input capacitance	$C_{In}$	—	6	pF
Control input capacitance	$C_{In}$	—	6	pF
Input/output capacitance	$C_{I/O}$	—	8	pF

NOTES:

<sup>1</sup>  $f = 1.0 \text{ MHz}$ ,  $dV = 3.0 \text{ V}$ ,  $T_A = 25^\circ C$ , periodically sampled rather than 100% tested.

Table 8. ac Measurement Conditions

Parameter	Value
Logic input timing measurement reference level	1.5 V
Logic output timing measurement reference level	1.5 V
Logic input pulse levels	0 or 3.0 V
Input rise/fall time	2 ns
Output load for low and high impedance parameters	See Figure 3A
Output load for all other timing parameters	See Figure 3B

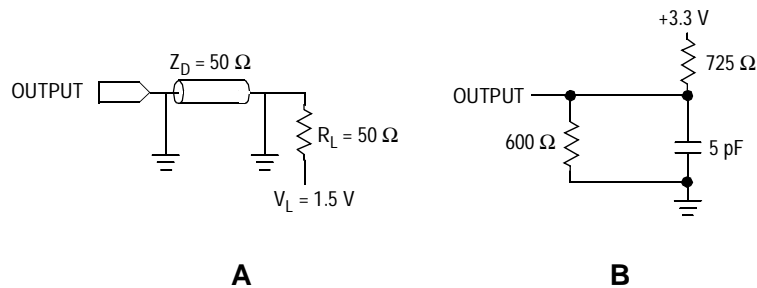


Figure 3. Output Load for ac Test

## Timing Specifications

### Read Mode

**Table 9. Read Cycle Timing<sup>1, 2</sup>**

Parameter	Symbol	Min	Max	Unit
Read cycle time	$t_{AVAV}$	35	—	ns
Address access time	$t_{AVQV}$	—	35	ns
Enable access time <sup>3</sup>	$t_{ELQV}$	—	35	ns
Output enable access time	$t_{GLQV}$	—	15	ns
Byte enable access time	$t_{BLQV}$	—	15	ns
Output hold from address change	$t_{AXQX}$	3	—	ns
Enable low to output active <sup>4, 5</sup>	$t_{ELQX}$	3	—	ns
Output enable low to output active <sup>4, 5</sup>	$t_{GLQX}$	0	—	ns
Byte enable low to output active <sup>4, 5</sup>	$t_{BLQX}$	0	—	ns
Enable high to output Hi-Z <sup>4, 5</sup>	$t_{EHQZ}$	0	15	ns
Output enable high to output Hi-Z <sup>4, 5</sup>	$t_{GHQZ}$	0	10	ns
Byte high to output Hi-Z <sup>4, 5</sup>	$t_{BHQZ}$	0	10	ns

**NOTES:**

- <sup>1</sup>  $\bar{W}$  is high for read cycle.
- <sup>2</sup> Due to product sensitivities to noise, power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read and write cycles.
- <sup>3</sup> Addresses valid before or at the same time  $\bar{E}$  goes low.
- <sup>4</sup> This parameter is sampled and not 100% tested.
- <sup>5</sup> Transition is measured  $\pm 200$  mV from steady-state voltage.





## Write Mode

Table 10. Write Cycle Timing 1 ( $\overline{W}$  Controlled)<sup>1, 2, 3, 4, 5</sup>

Parameter	Symbol	Min	Max	Unit
Write cycle time <sup>6</sup>	$t_{AVAV}$	35	—	ns
Address set-up time	$t_{AVWL}$	0	—	ns
Address valid to end of write ( $\overline{G}$ high)	$t_{AVWH}$	18	—	ns
Address valid to end of write ( $\overline{G}$ low)	$t_{AVWH}$	20	—	ns
Write pulse width ( $\overline{G}$ high)	$t_{WLWH}$ $t_{WLEH}$	15	—	ns
Write pulse width ( $\overline{G}$ low)	$t_{WLWH}$ $t_{WLEH}$	15	—	ns
Data valid to end of write	$t_{DVWH}$	10	—	ns
Data hold time	$t_{WHDX}$	0	—	ns
Write low to data Hi-Z <sup>7, 8, 9</sup>	$t_{WLQZ}$	0	12	ns
Write high to output active <sup>7, 8, 9</sup>	$t_{WHQX}$	3	—	ns
Write recovery time	$t_{WHAX}$	12	—	ns

## NOTES:

- <sup>1</sup> A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
- <sup>2</sup> Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
- <sup>3</sup> If  $\overline{G}$  goes low at the same time or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
- <sup>4</sup> After  $\overline{W}$ ,  $\overline{E}$ , or  $\overline{UB/LB}$  has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- <sup>5</sup> The minimum time between  $\overline{E}$  being asserted low in one cycle to  $\overline{E}$  being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- <sup>6</sup> All write cycle timings are referenced from the last valid address to the first transition address.
- <sup>7</sup> This parameter is sampled and not 100% tested.
- <sup>8</sup> Transition is measured  $\pm 200$  mV from steady-state voltage.
- <sup>9</sup> At any given voltage or temperature,  $t_{WLQZ} \text{ max} < t_{WHQX} \text{ min}$ .

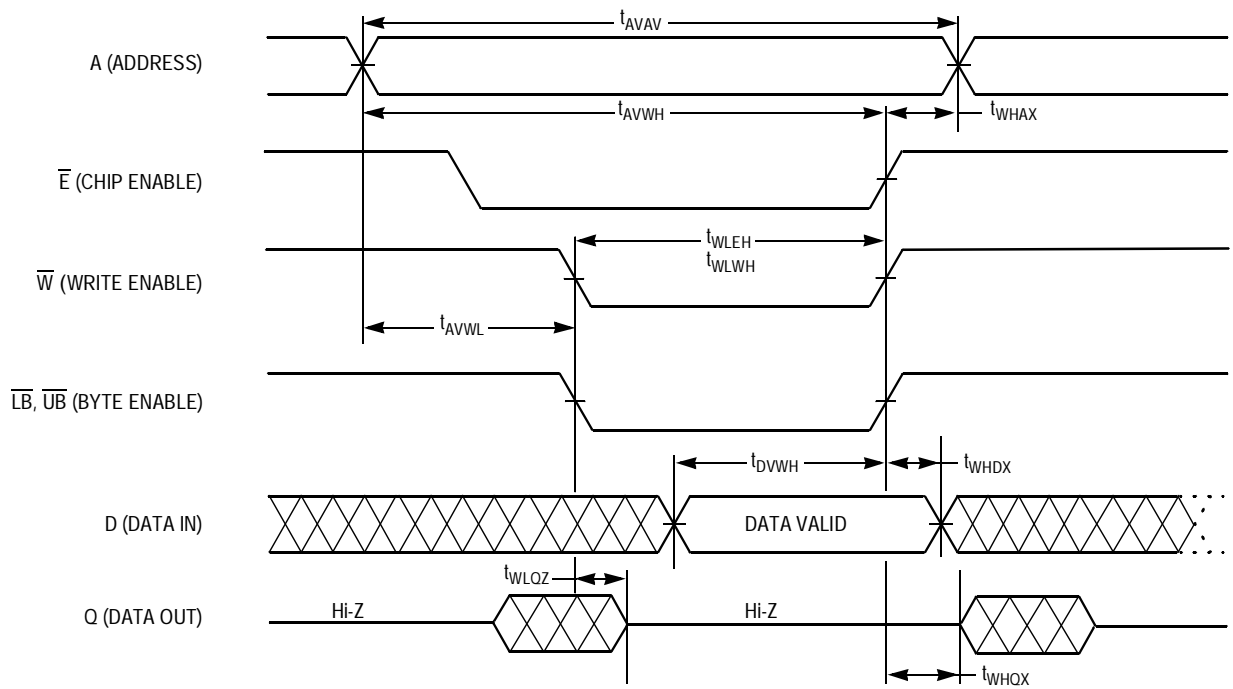


Figure 6. Write Cycle 1 ( $\overline{W}$  Controlled)

Table 11. Write Cycle Timing 2 ( $\overline{E}$  Controlled)<sup>1, 2, 3, 4, 5</sup>

Parameter	Symbol	Min	Max	Unit
Write cycle time <sup>6</sup>	$t_{AVAV}$	35	—	ns
Address set-up time	$t_{AVEL}$	0	—	ns
Address valid to end of write ( $\overline{G}$ high)	$t_{AVEH}$	18	—	ns
Address valid to end of write ( $\overline{G}$ low)	$t_{AVEH}$	20	—	ns
Enable to end of write ( $\overline{G}$ high)	$t_{ELEH}$ $t_{ELWH}$	15	—	ns
Enable to end of write ( $\overline{G}$ low) <sup>7, 8</sup>	$t_{ELEH}$ $t_{ELWH}$	15	—	ns
Data valid to end of write	$t_{DVEH}$	10	—	ns
Data hold time	$t_{EHDX}$	0	—	ns
Write recovery time	$t_{EHAX}$	12	—	ns

## NOTES:

- <sup>1</sup> A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
- <sup>2</sup> Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
- <sup>3</sup> If  $\overline{G}$  goes low at the same time or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
- <sup>4</sup> After  $\overline{W}$ ,  $\overline{E}$ , or  $\overline{UB/LB}$  has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- <sup>5</sup> The minimum time between  $\overline{E}$  being asserted low in one cycle to  $\overline{E}$  being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- <sup>6</sup> All write cycle timings are referenced from the last valid address to the first transition address.
- <sup>7</sup> If  $\overline{E}$  goes low at the same time or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.
- <sup>8</sup> If  $\overline{E}$  goes high at the same time or before  $\overline{W}$  goes high, the output will remain in a high-impedance state.

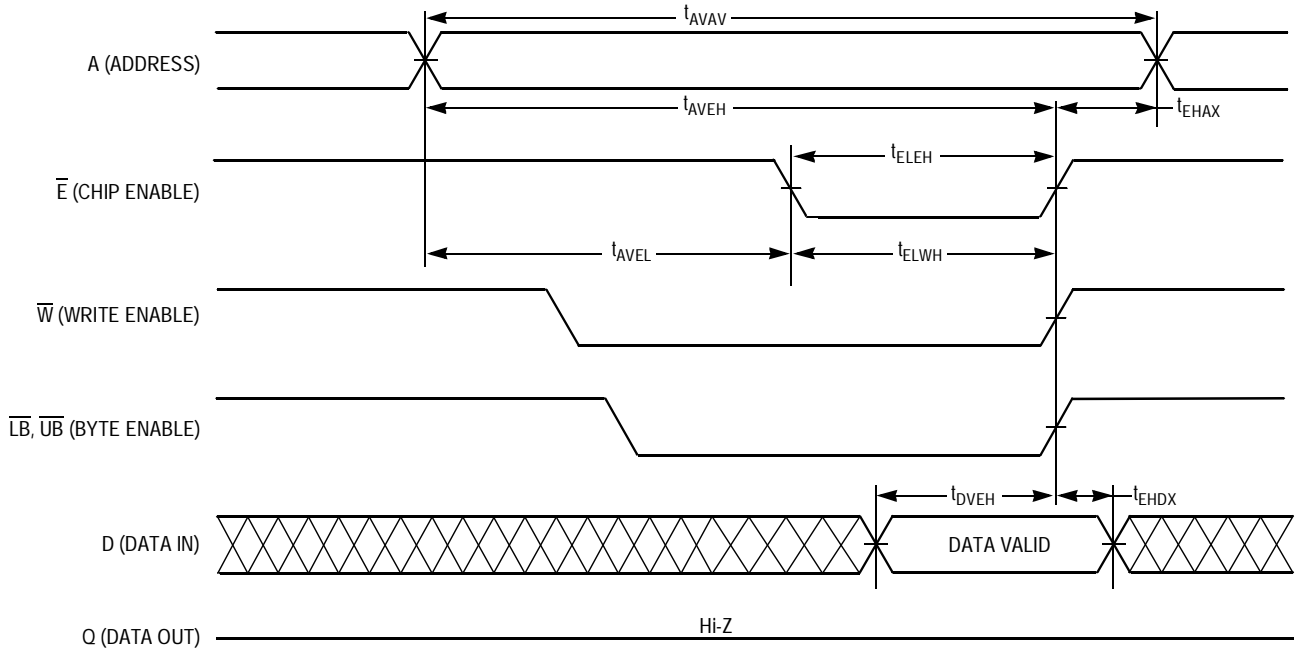


Figure 7. Write Cycle 2 ( $\bar{E}$  Controlled)

**Table 12. Write Cycle Timing 3 ( $\overline{\text{LB}}/\overline{\text{UB}}$  Controlled)<sup>1, 2, 3, 4, 5, 6</sup>**

Parameter	Symbol	Min	Max	Unit
Write cycle time <sup>7</sup>	$t_{\text{AVAV}}$	35	—	ns
Address set-up time	$t_{\text{AVBL}}$	0	—	ns
Address valid to end of write ( $\overline{\text{G}}$ high)	$t_{\text{AVBH}}$	18	—	ns
Address valid to end of write ( $\overline{\text{G}}$ low)	$t_{\text{AVBH}}$	20	—	ns
Byte pulse width ( $\overline{\text{G}}$ high)	$t_{\text{BLEH}}$ $t_{\text{BLWH}}$	15	—	ns
Byte pulse width ( $\overline{\text{G}}$ low)	$t_{\text{BLEH}}$ $t_{\text{BLWH}}$	15	—	ns
Data valid to end of write	$t_{\text{DVBH}}$	10	—	ns
Data hold time	$t_{\text{BHDX}}$	0	—	ns
Write recovery time	$t_{\text{BHAX}}$	12	—	ns

## NOTES:

- <sup>1</sup> A write occurs during the overlap of  $\overline{\text{E}}$  low and  $\overline{\text{W}}$  low.
- <sup>2</sup> Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
- <sup>3</sup> If  $\overline{\text{G}}$  goes low at the same time or after  $\overline{\text{W}}$  goes low, the output will remain in a high-impedance state.
- <sup>4</sup> After  $\overline{\text{W}}$ ,  $\overline{\text{E}}$ , or  $\overline{\text{UB}}/\overline{\text{LB}}$  has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- <sup>5</sup> If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them.
- <sup>6</sup> The minimum time between  $\overline{\text{E}}$  being asserted low in one cycle to  $\overline{\text{E}}$  being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- <sup>7</sup> All write cycle timings are referenced from the last valid address to the first transition address.

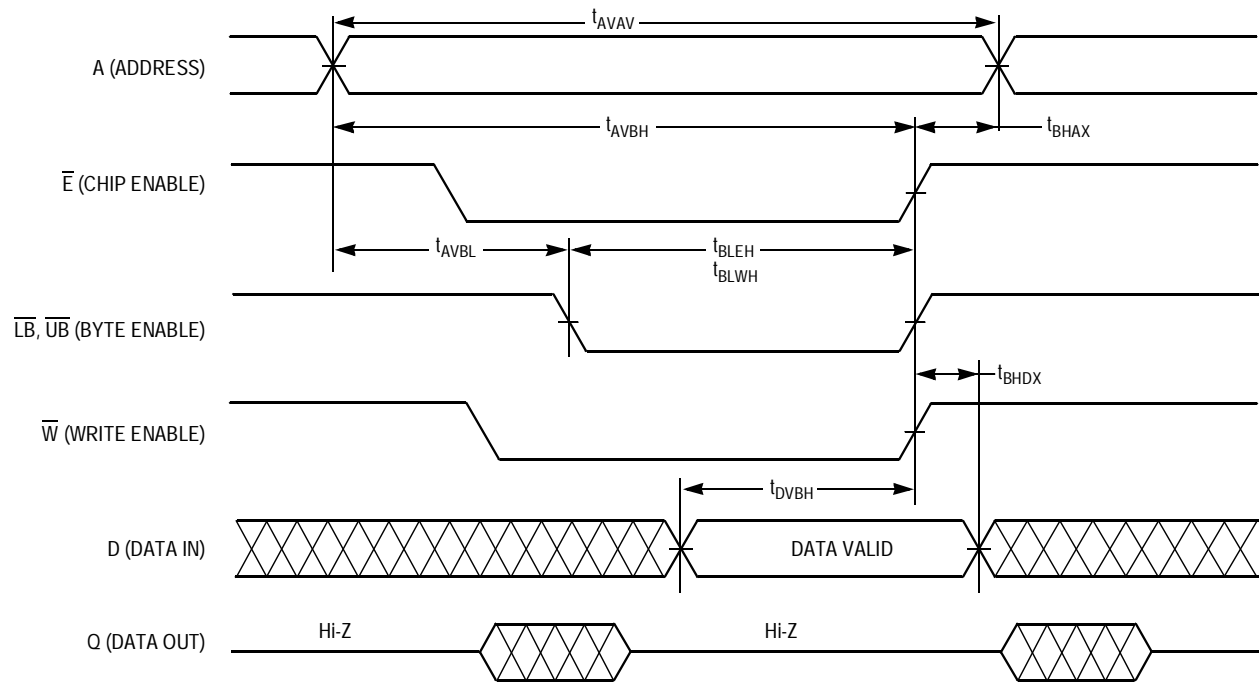


Figure 8. Write Cycle 3 ( $\overline{LB}/\overline{UB}$  Controlled)

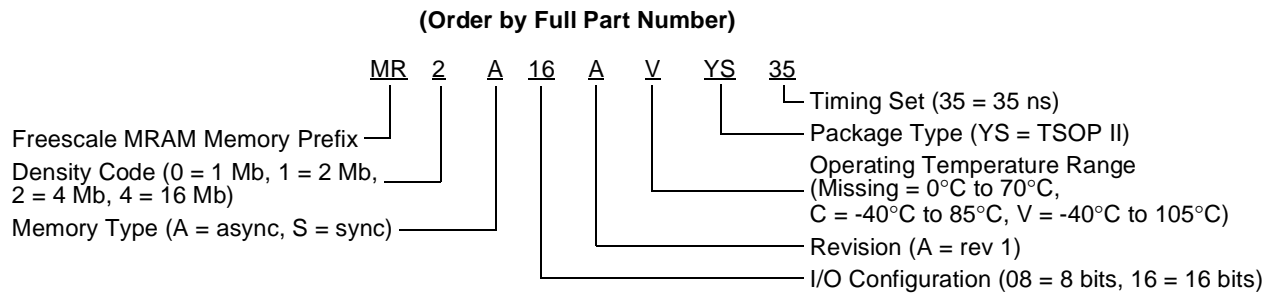
## Ordering Information

This product is available in Commercial, Industrial, and Extended temperature versions.

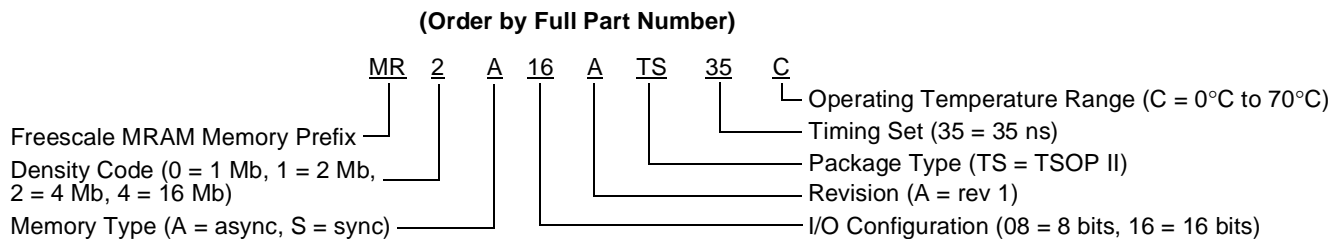
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- **Industrial, Extended** — Typically 10 year applications - installed telecom equipment, workstations, servers, etc. These products can also be used in Commercial applications.

### Current Part Numbering System (New Commercial, Industrial and Extended devices)



### Legacy Part Numbering System (Legacy Commercial devices)





## Package Information

**Table 13. Package Information**

Device	Pin Count	Package Type	Designator	Case No.	Document No.	RoHS Compliant
MR2A16A	44	TSOP Type II	TS/YS <sup>1</sup>	924A-02	98ASS23673W	True

NOTES:

- <sup>1</sup> TS and YS are both valid package codes for TSOP packages. The package is identical for both TS and YS codes.

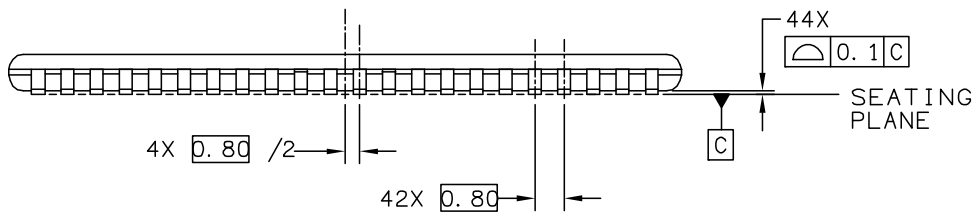
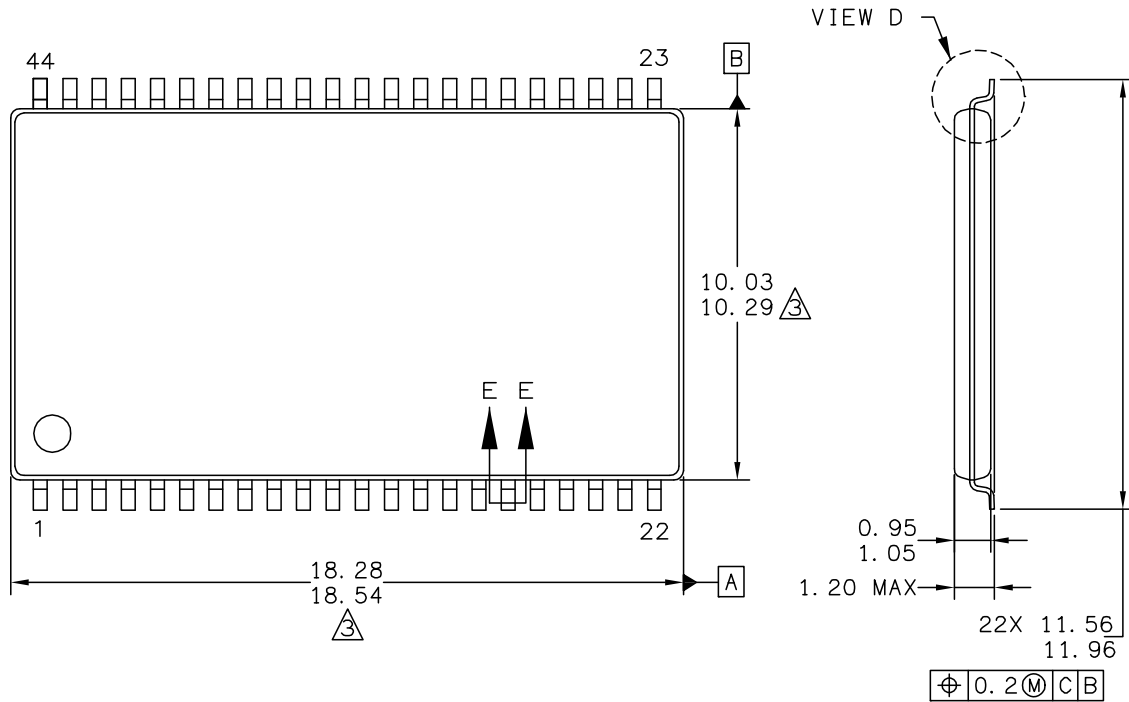
## Revision History

### Revision History

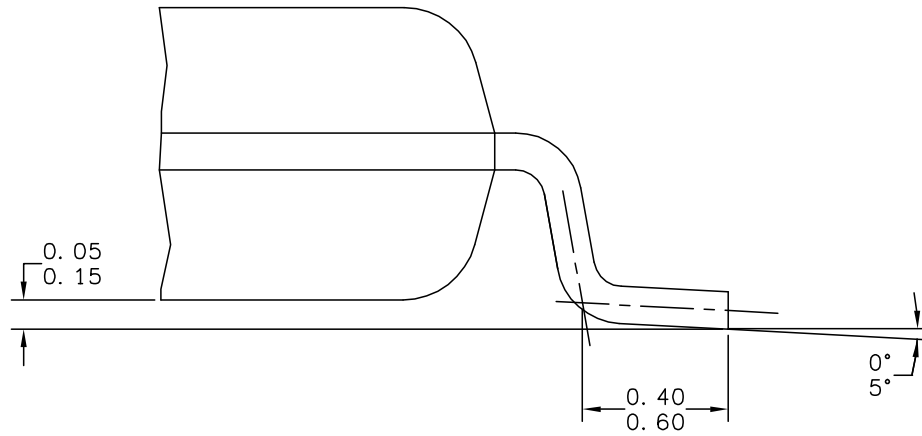
Revision	Date	Description of Change
4	18 Jun 2007	Added new Industrial and Extended temperature product information; updated part ordering information; changed to 2 ms delay after power up; power supply characteristics values updated to TBD for industrial and extended temperature devices.
5	21 Sep 2007	Changed MR2A16ATS35C product description to Legacy Commercial. Added the New Commercial temperature product (MR2A16AYS35) information. Table 3: MR2A16AYS35 $H_{\max\_write} = 25$ Oe. Table 4: MR2A16AYS35 has a 2 ms power up waiting period. Table 6: Applied values to TBD's in IDD specifications.
6	12 Nov 2007	Table 2: Changed IDDA to IDDR or IDDW. Table 13: Added note indicating that TS and YS are both valid package codes. Current Part Numbering System: Added commercial (missing letter) temperature range.

## Mechanical Drawing

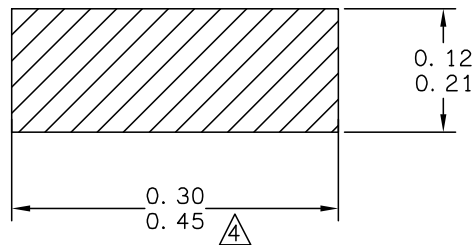
The following pages detail the package available to MR2A16A.



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	STANDARD: NON-JEDEC		



VIEW D  
ROTATED 90° CW



SECTION E-E  
40 PLACES

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	CASE NUMBER: 924A-02	17 MAY 2005	
STANDARD: NON-JEDEC			

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M – 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.  
ALLOWABLE MOLD PROTRUSION IS 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSIONS.  
DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH  
TO EXCEED 0.58.

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